

FIG.1 PRIOR ART

FIG. 2 PRIOR ART

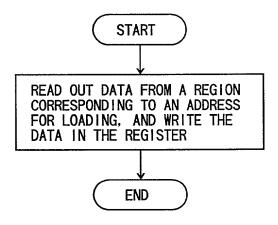


FIG. 3 PRIOR ART

OP-CODE	GR1	GR2	GRD

FIG. 4 PRIOR ART

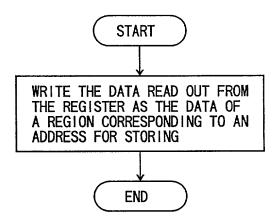
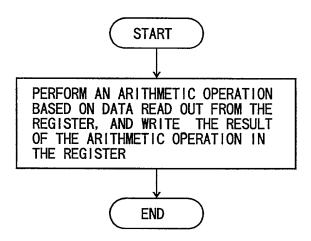


FIG. 5 PRIOR ART

OP-CODE	GR1	GR2	GRS
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INTERRUPT CONTROL CIRCUIT 0 ∞ 30 EPSR 33 INTERRUPT SIGNAL FLOATING POINT REGISTER INTERRUPT SIGNAL GENERAL REGISTER 39 37 CONDITION EPCR PSR 31 FIG.6 PRIOR ART က } တ် INSTRUCTION EXECUTION CIRCUIT 23 ~29 FLOATING POINT ARITHMETIC OPERATION INSTRUCTION EXECUTION UNIT ARITHMETIC OPERATION INSTRUCTION EXECUTION UNIT # PC 22 5 STORE INSTRUCTION EXECUTION UNIT FLOATING POINT STORE INSTRUCTION EXECUTION UNIT 2 27 INSTRUCTION READ CONTROL UNIT INSTRUCTION EXECUTION UNIT INSTRUCTION EXECUTION UNIT FLOATING POINT LOAD LOAD 9 INSTRUCTION F 25 α 2 DATA STORE DATA LOAD **MEMORY**

FIG. 7 PRIOR ART



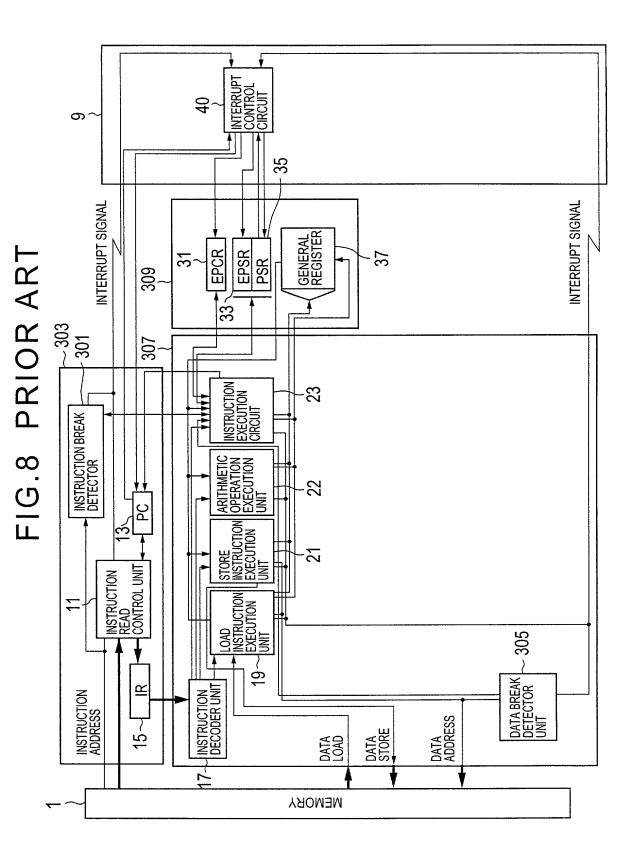
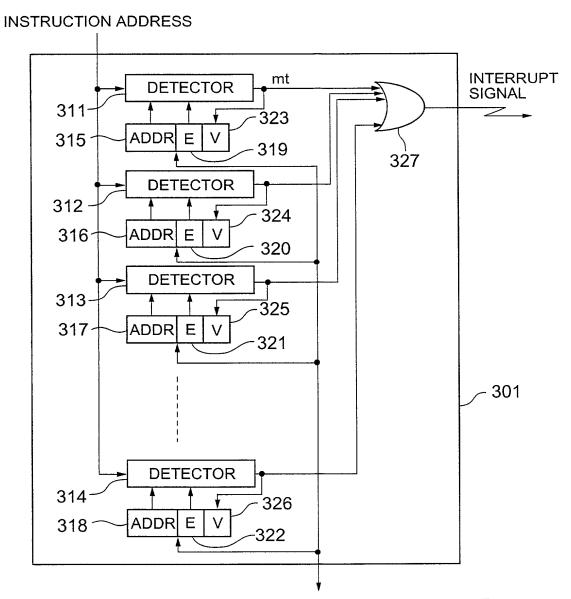
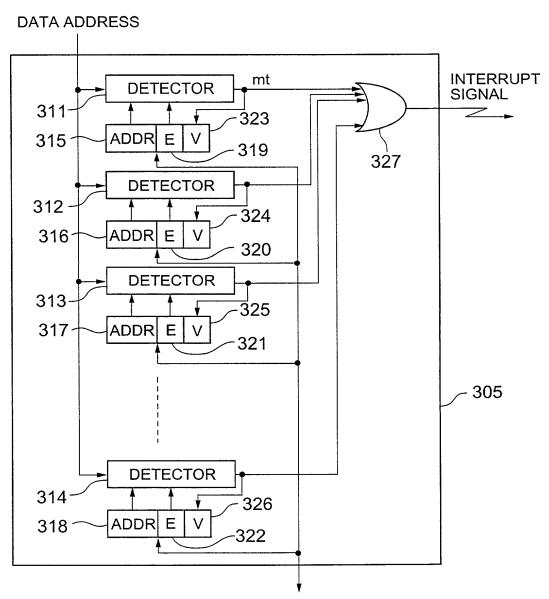


FIG.9 PRIOR ART



TO THE INSTRUCTION EXECUTION CIRCUIT

FIG.10 PRIOR ART



TO THE INSTRUCTION EXECUTION CIRCUIT

FIG.11 PRIOR ART

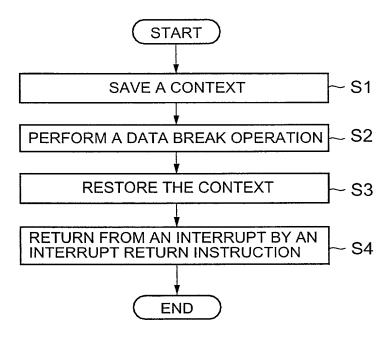


FIG.12 PRIOR ART

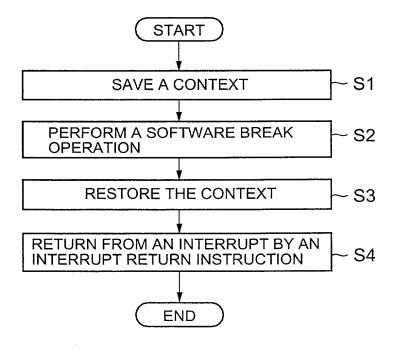
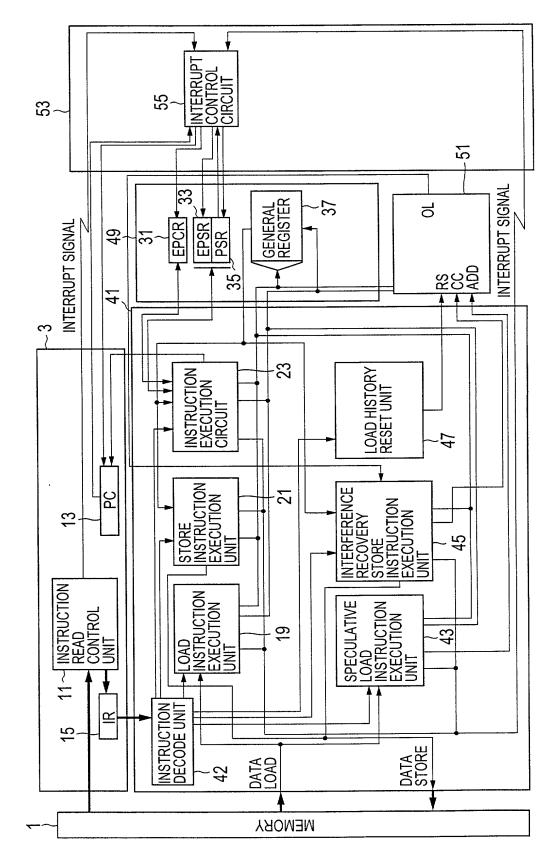


FIG.13



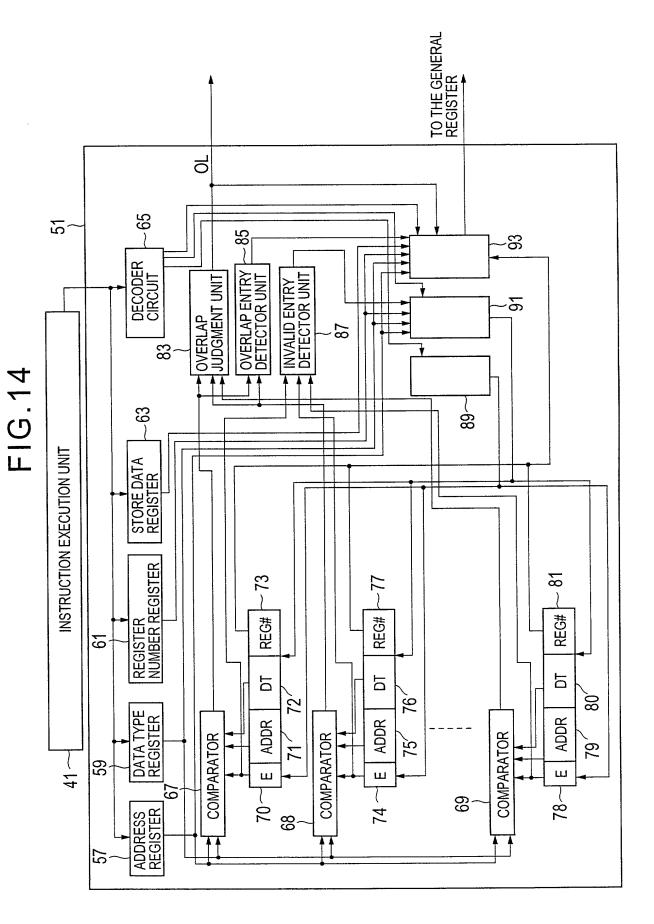


FIG. 15

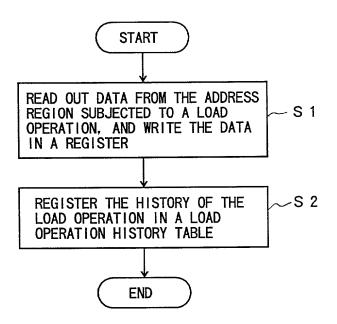


FIG. 16

OP-CODE	GR1	GR2	GRD
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FIG. 17

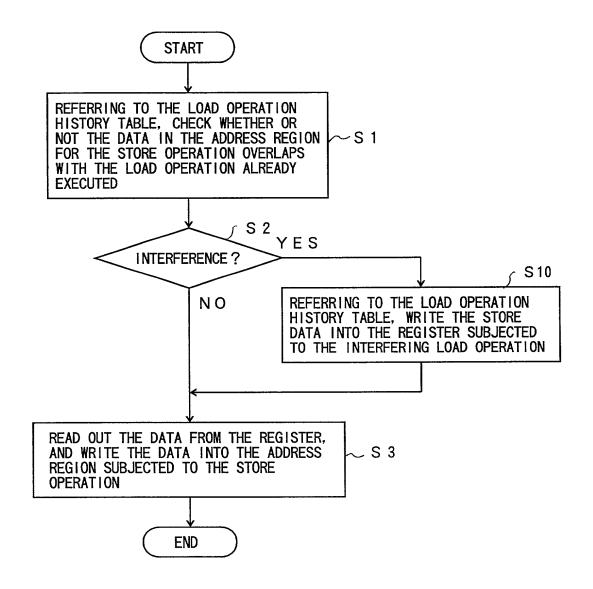


FIG. 18

OP-CODE	GR1	GR2	GRS

FIG. 19

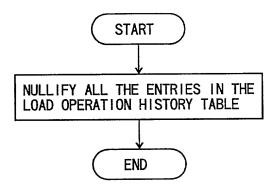
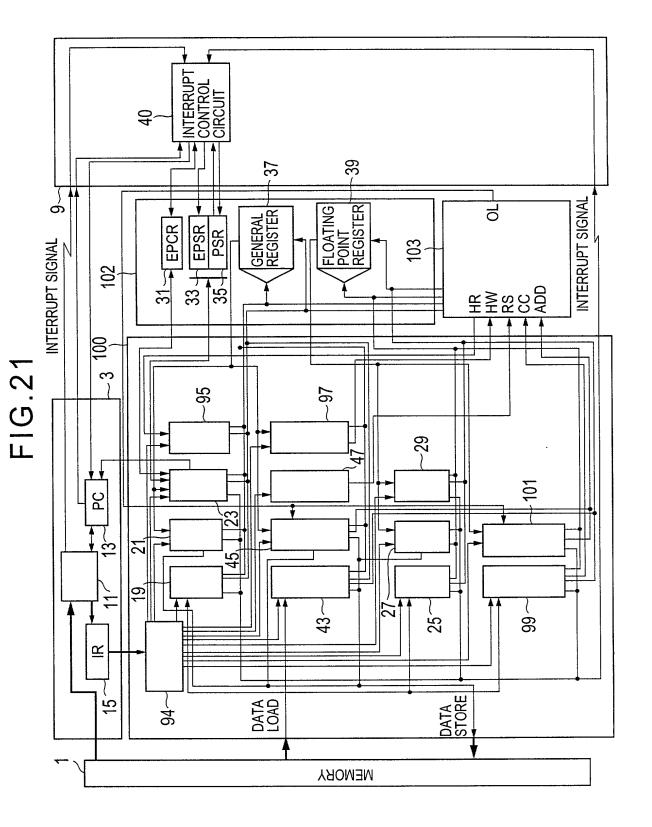
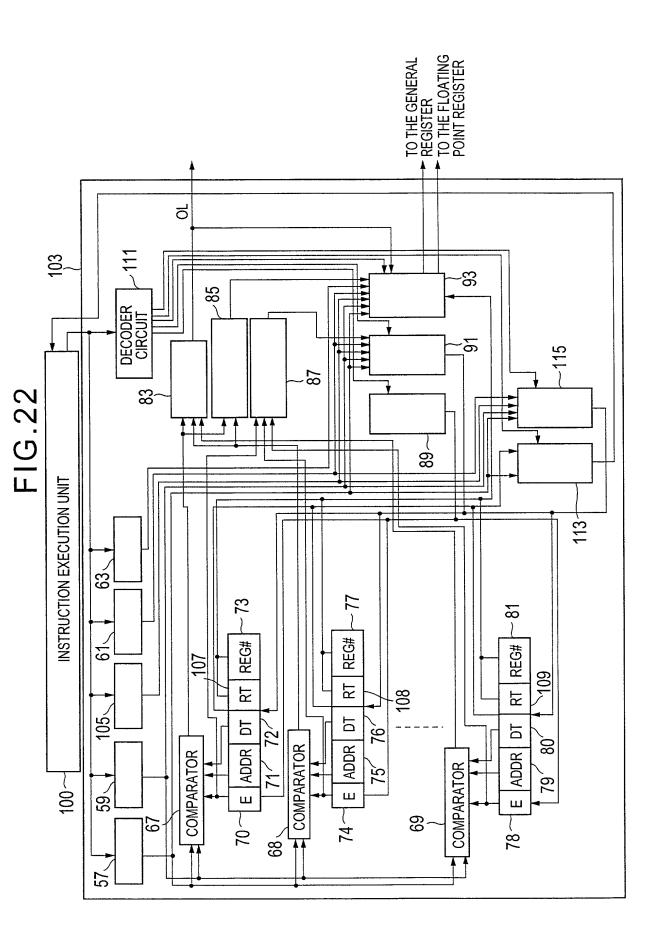
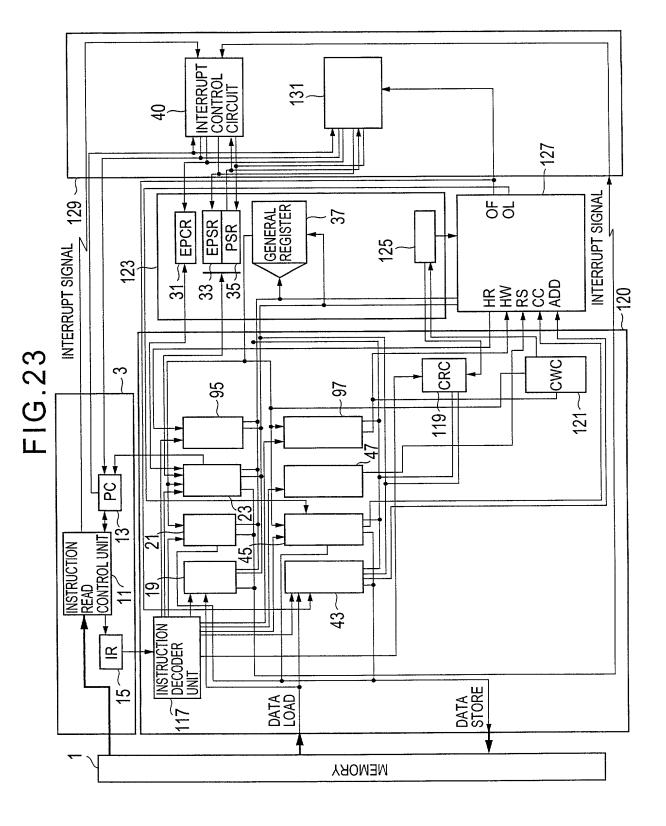


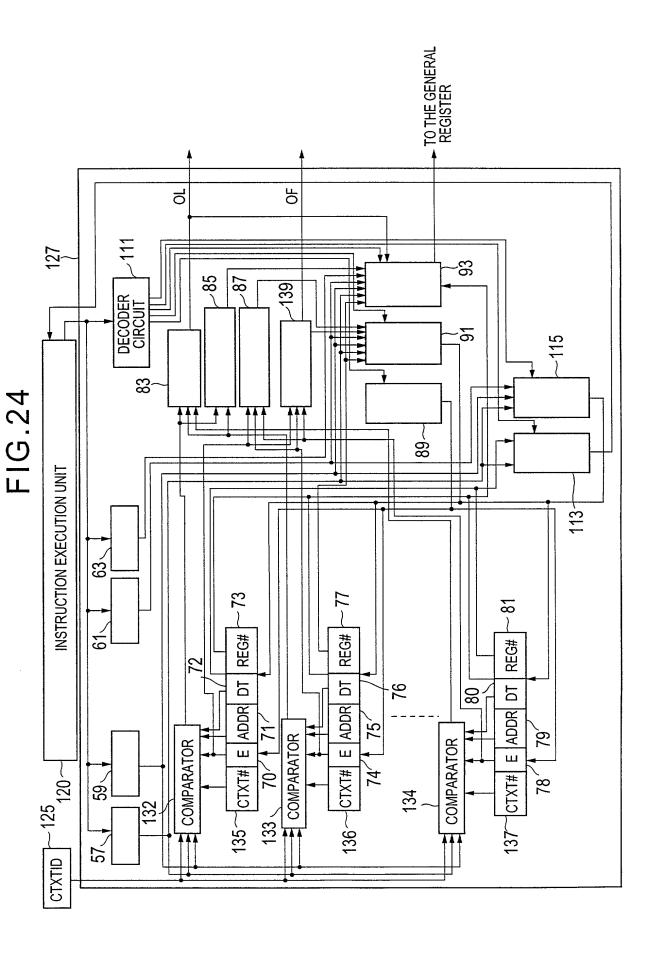
FIG. 20

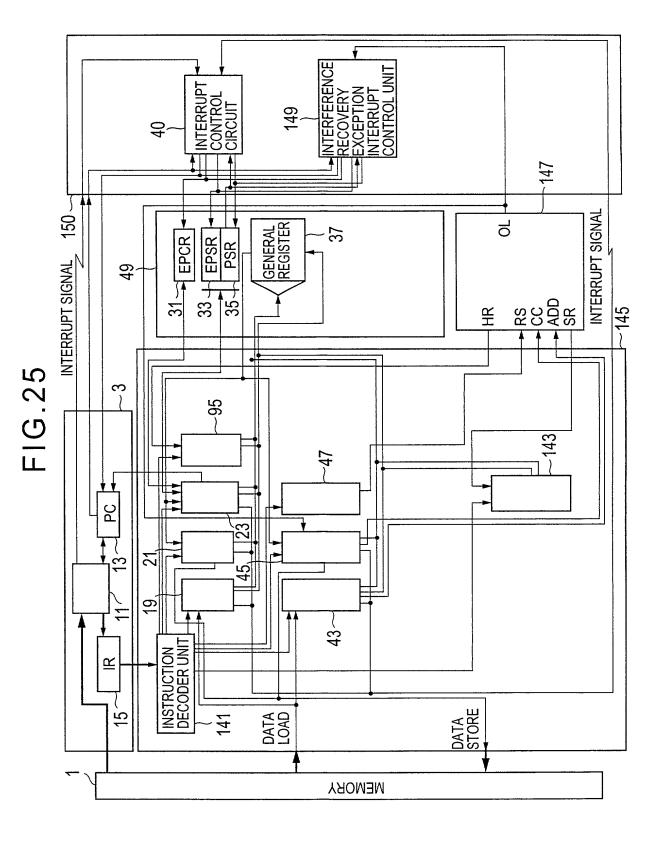
	 		l
OP-CODE	 		











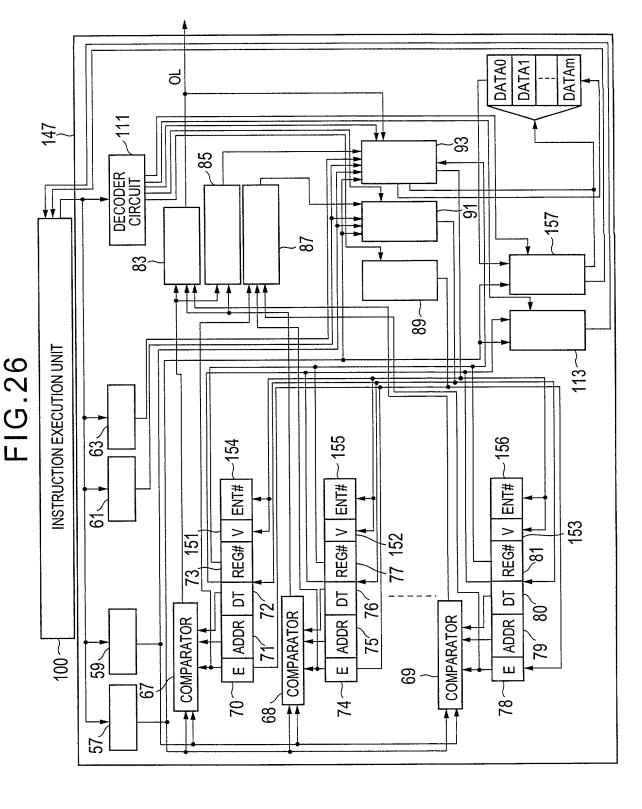


FIG. 27

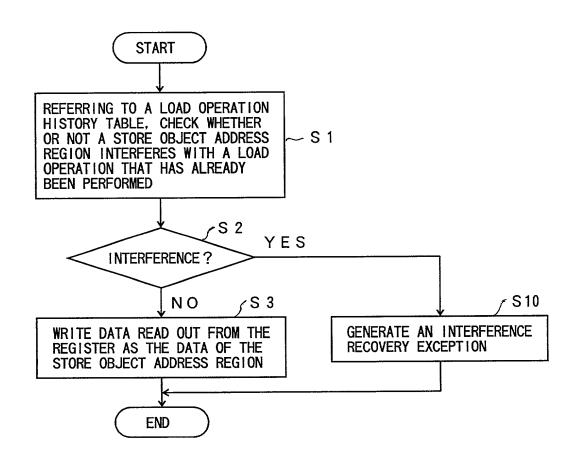
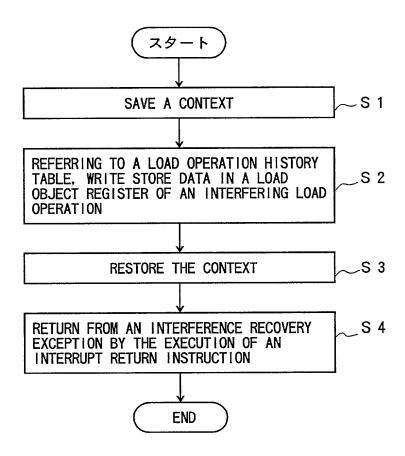
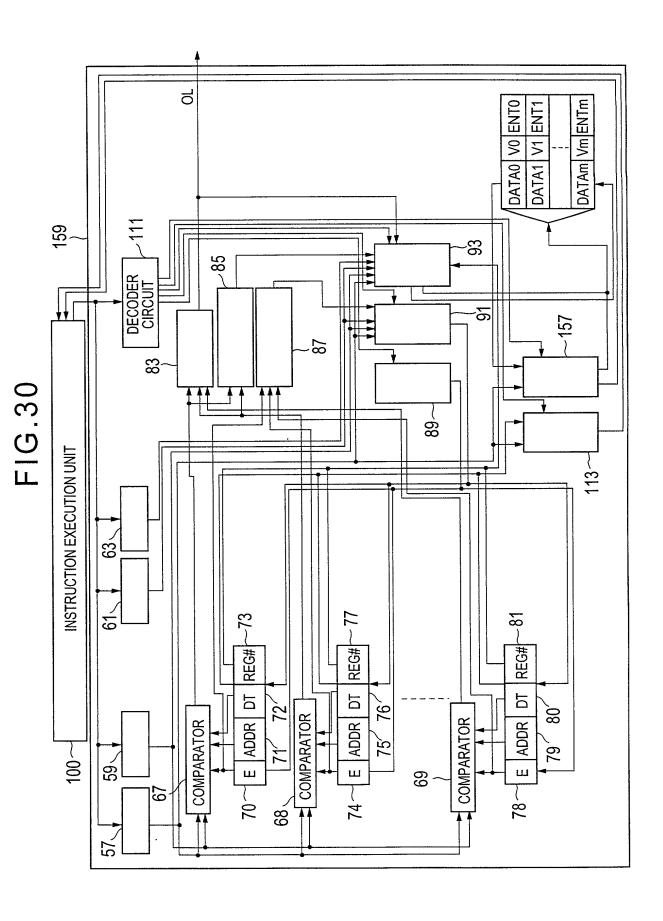


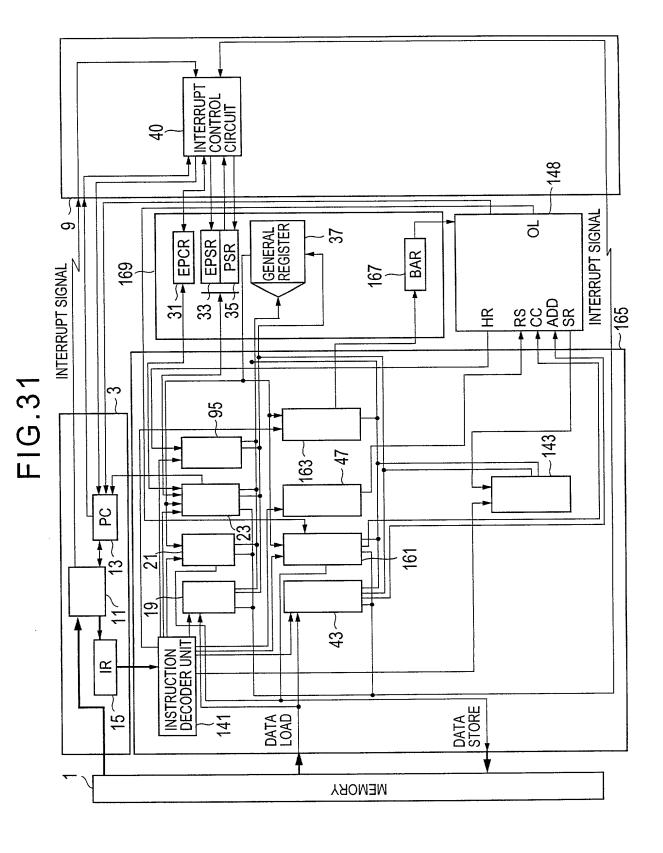
FIG. 28

OP-CODE	GR1	GR2	GRS

FIG. 29







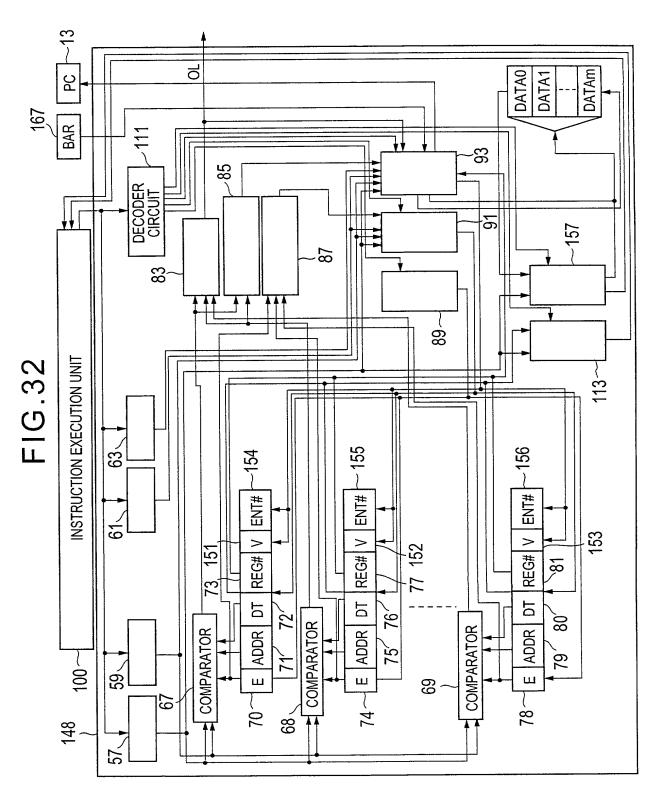


FIG. 33

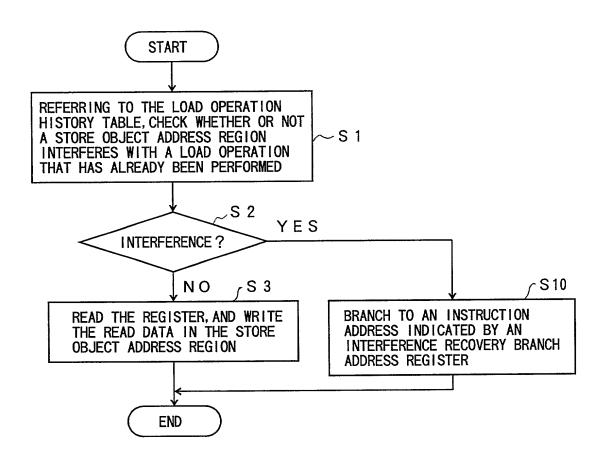


FIG. 34

OP-CODE	GR1	GR2	GRS

INTERRUPT CONTROL CIRCUIT 4 10 INTERRUPT SIGNAL 38 $\mathbb{C}^{\mathbb{N}}$ CONDITION CNEK 33 → EPSR F EPCR 37 PSR INTERRUPT SIGNAL 35.∏ 30 ADD <u>~≥°</u> ~170 33 INSTRUCTION EXECUTION CIRCUIT \sim 20 $^{\mathsf{PC}}$ ~28 13 22 INSTRUCTION READ CONTROL UNIT 26 LOAD INSTRUCTION EXECUTION UNIT 24° 6 <u>K</u> INSTRUCTION DECODER UNIT 5 **MEMORY**

FIG.35

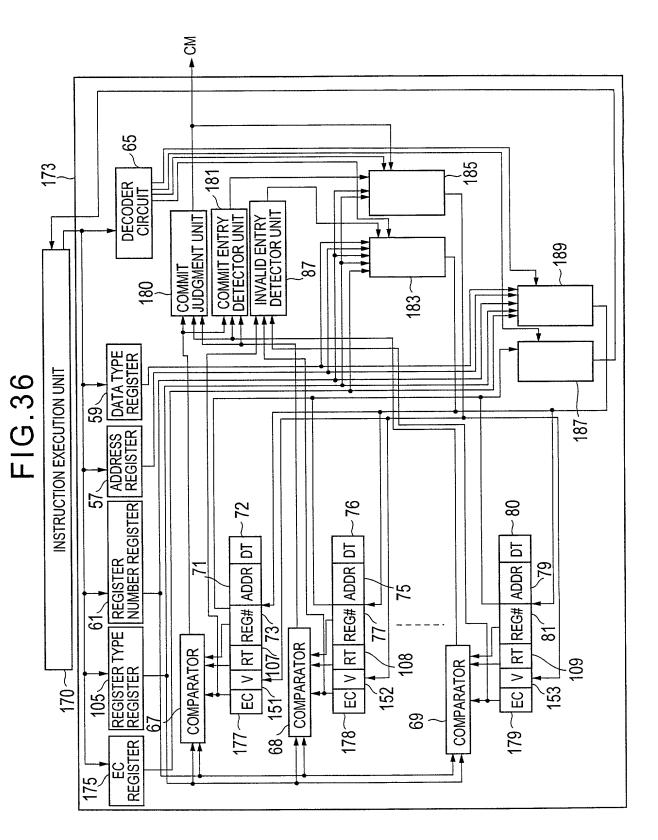


FIG. 37

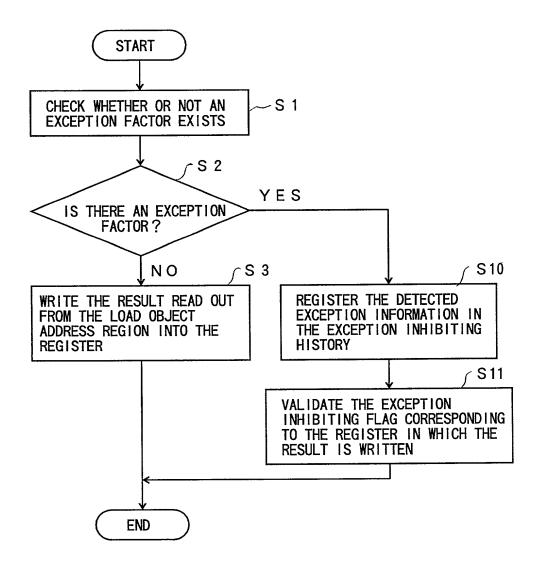


FIG. 38

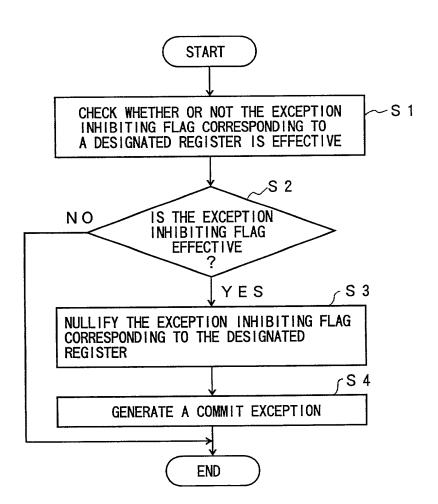
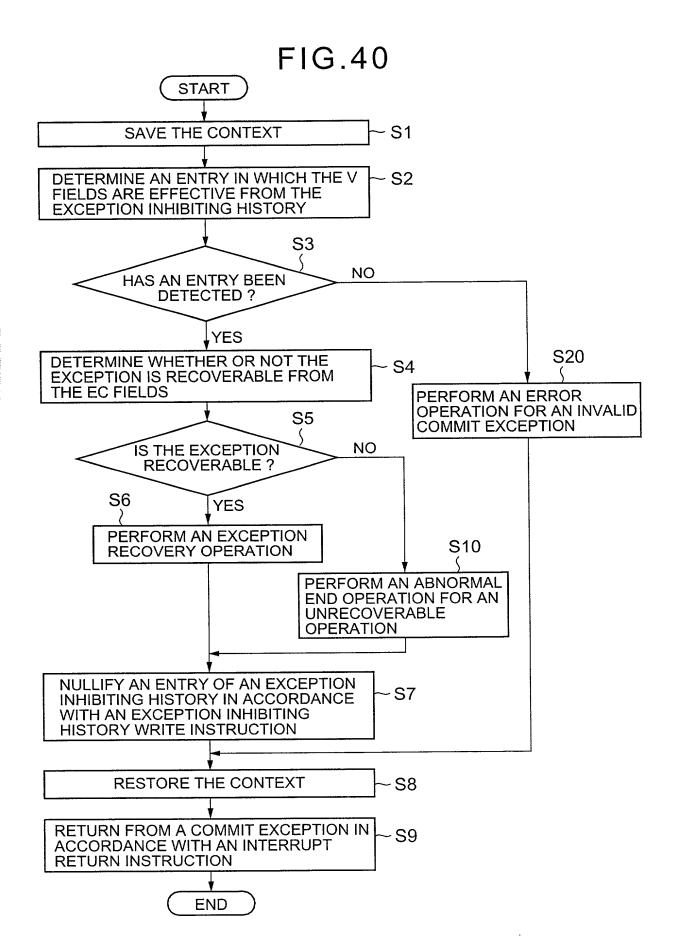
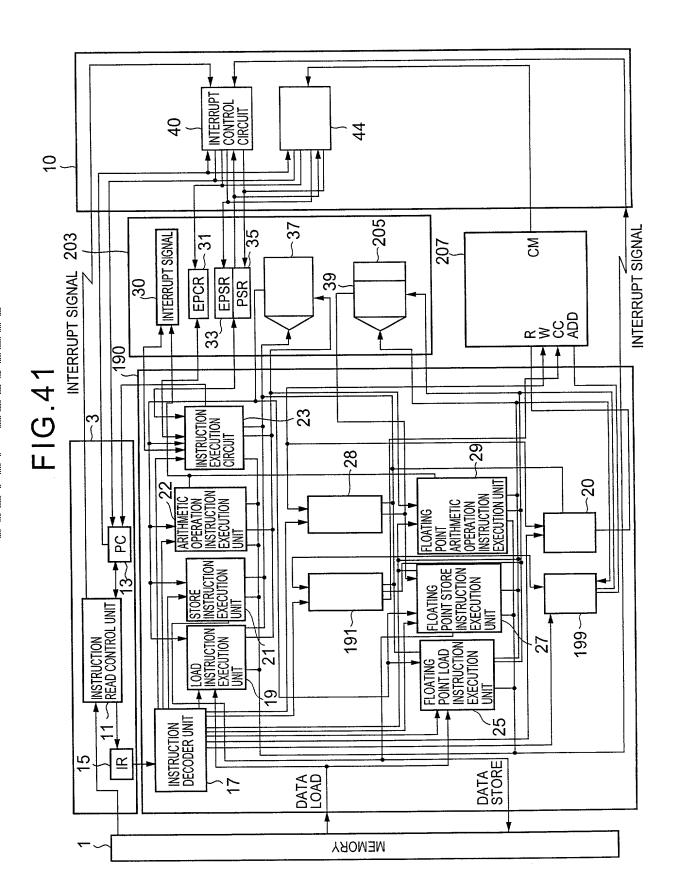


FIG. 39

OP-CODE	GR	
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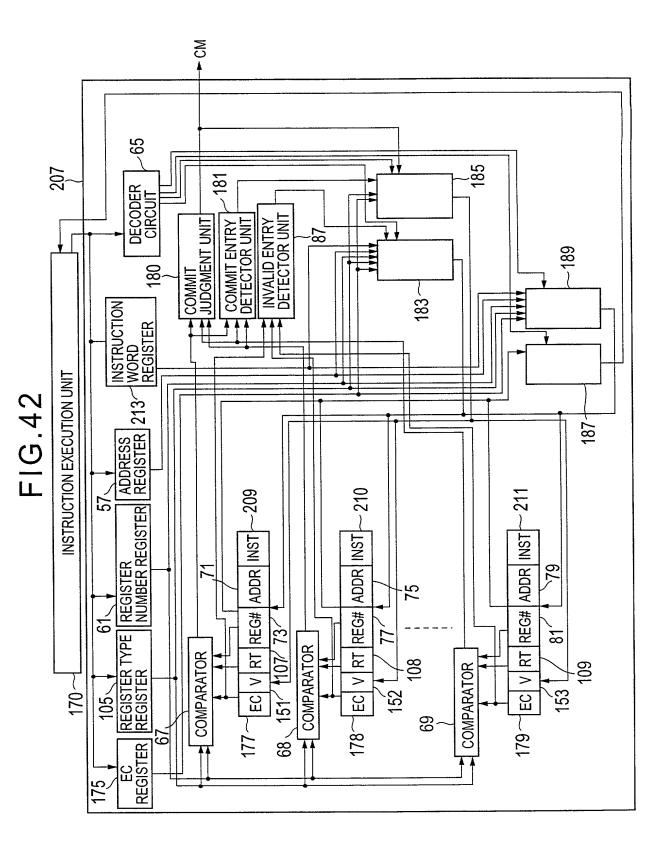
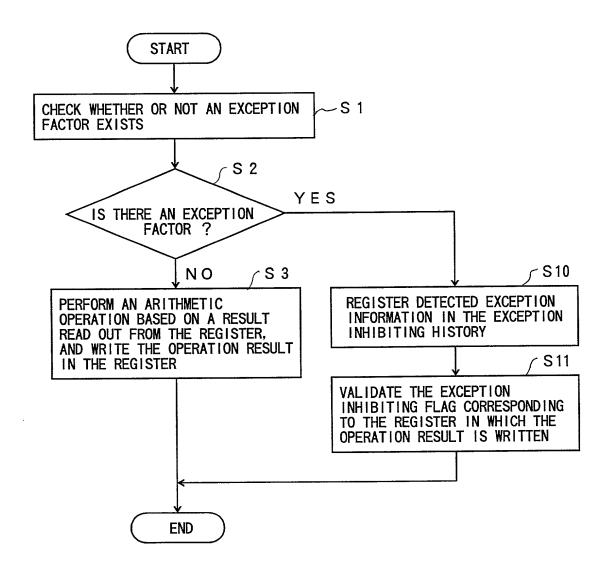
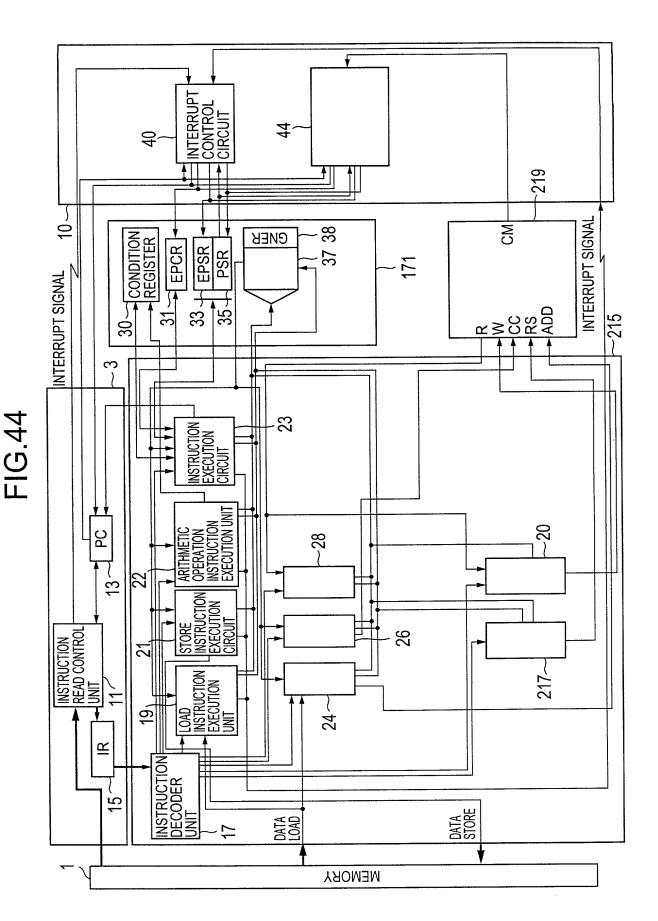


FIG. 43





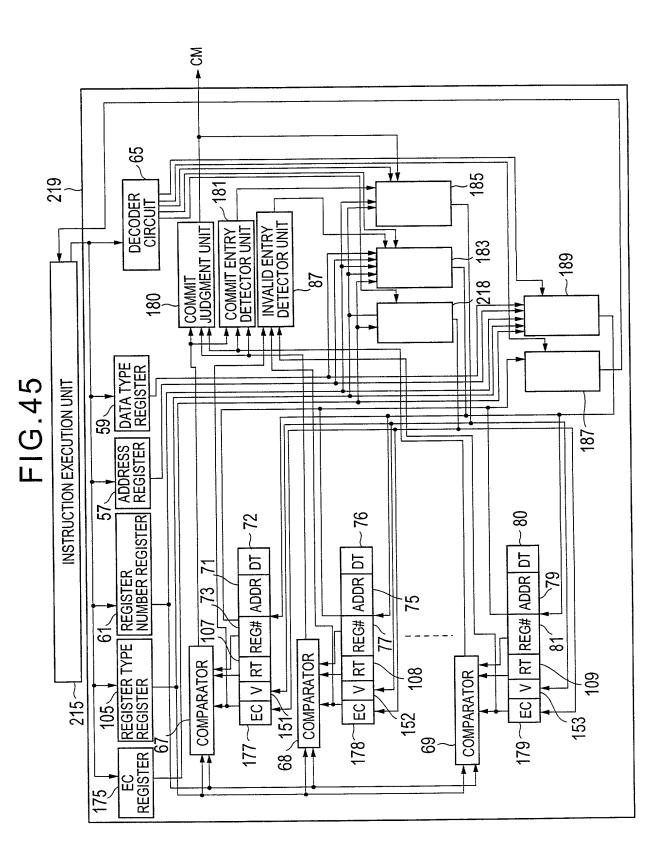
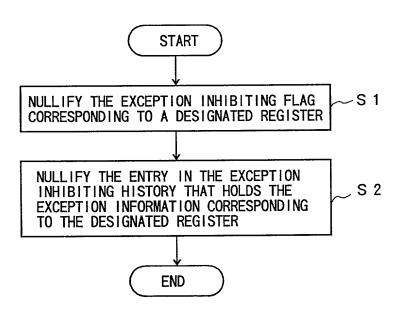
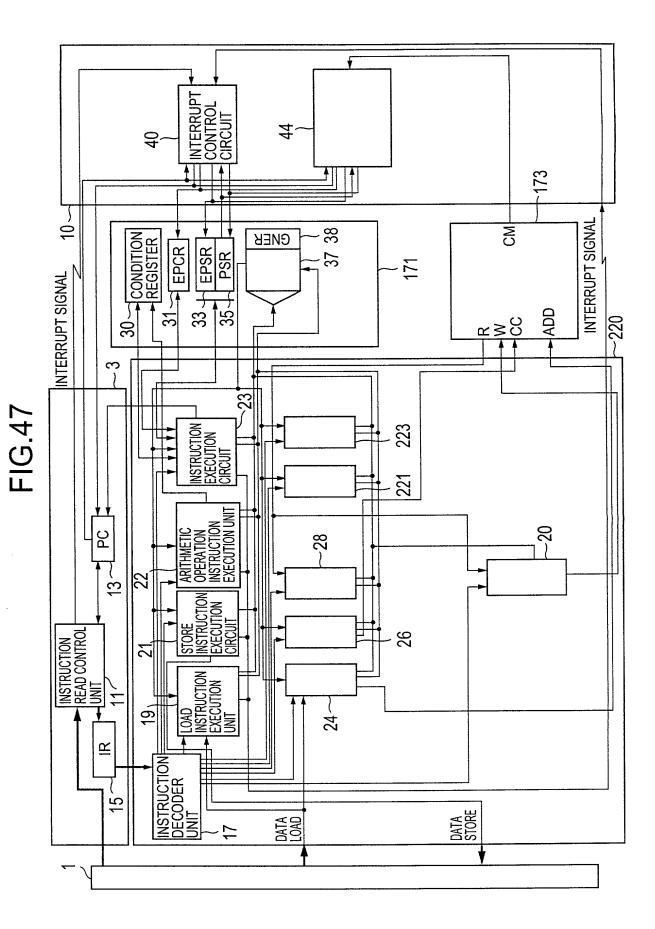
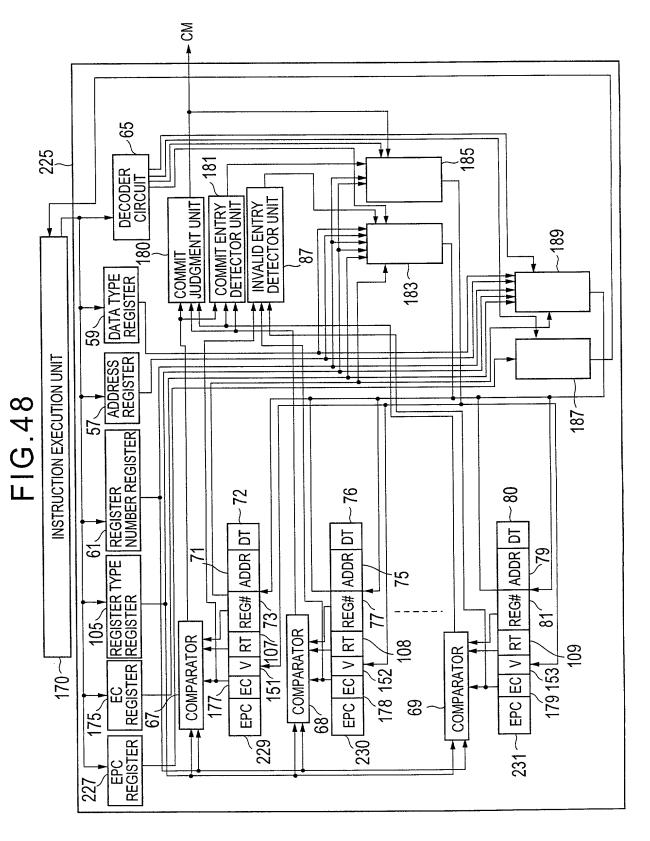
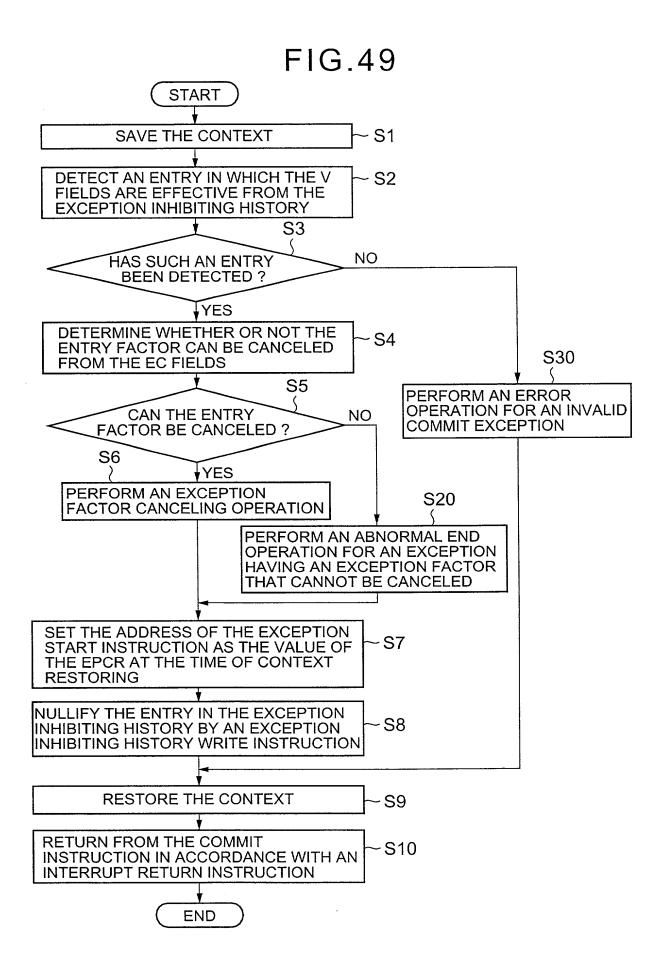


FIG. 46









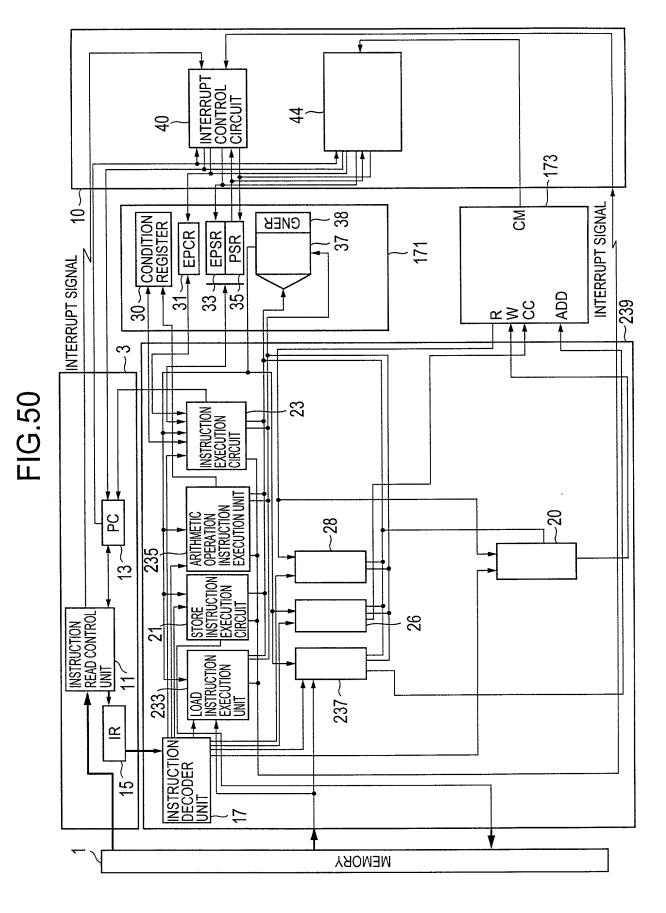


FIG. 51

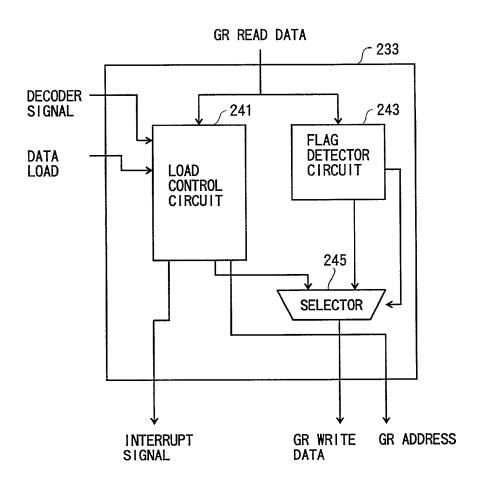


FIG. 52

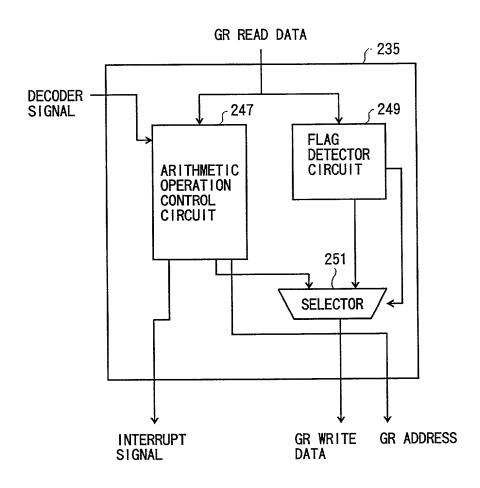


FIG. 53

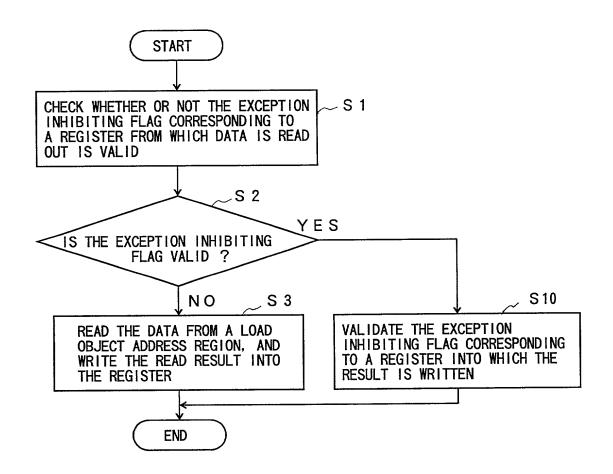


FIG. 54

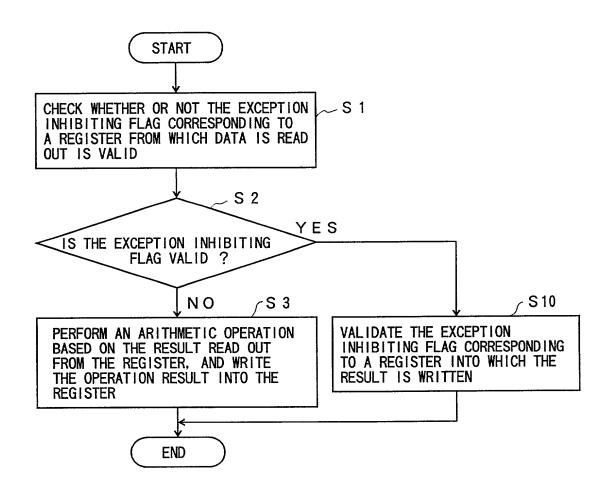
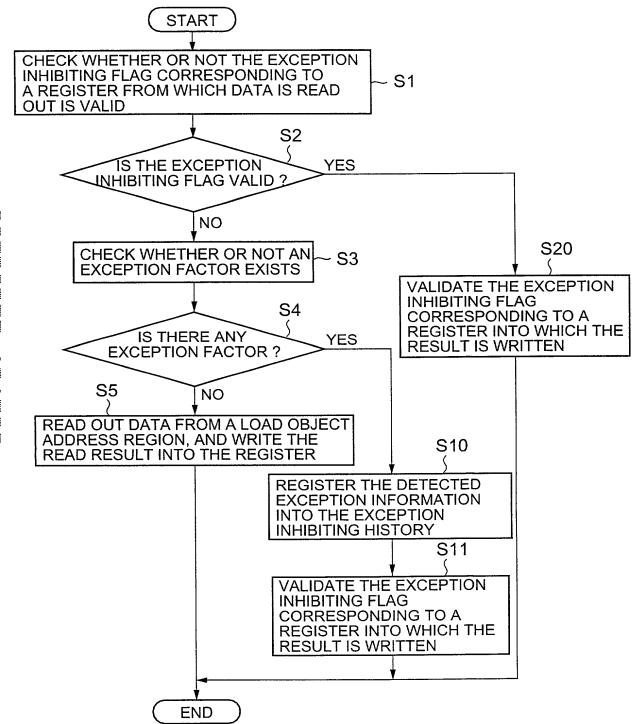


FIG.55



<u>တ</u> -331 35 INTERRUPT SIGNAL INTERRUPT SIGNAL CNEK 38 GENERAL REGISTER EPSR PSR EPCR 37 ~303 301 329 **************** INSTRUCTION EXECUTION CIRCUIT 23 INSTRUCTION BREAK DETECTOR UNIT ည STORE INSTRUCTION EXECUTION UNIT က် \sim 24 INSTRUCTION READ CONTROL UNIT 305 19~ DATA BREAK DETECTOR UNIT INSTRUCTION ADDRESS INSTRUCTION DECODER UNIT <u>~</u> DATA ADDRESS 15~ DATA STORE DATA LOAD **MEMORY**

FIG.56

FIG.57

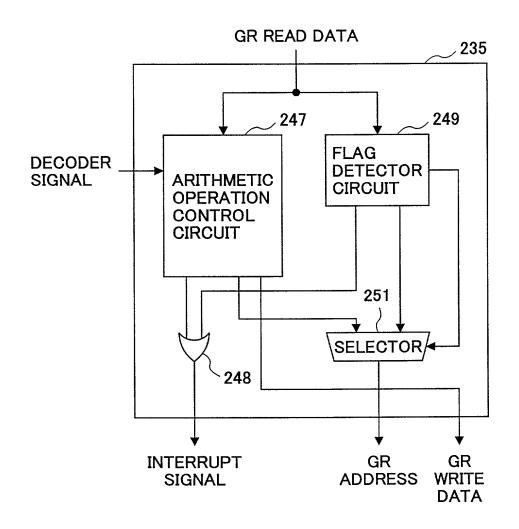


FIG.58

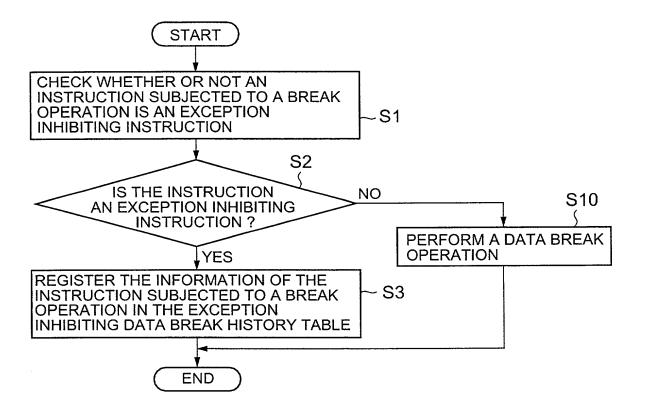


FIG.59 START CHECK WHETHER OR NOT A DATA BREAK IN A CONTROL PATH IN WHICH EXECUTION IS -S1 **ENSURED IS FOUND IN THE EXCEPTION** INHIBITING DATA BREAK HISTORY TABLE S2 YES IS THE DATA **S10 BREAK FOUND?** CHECK WHETHER OR NOT S3 NO ANOTHER CONTROL PATH **EXISTS** CHECK WHETHER OR NOT ANOTHER S11 **CONTROL PATH EXISTS S4** NO ANOTHER CONTROL PATH EXIST? NO ANOTHER CONTROL S12 PATH EXIST? YES YES NULLIFY THE INFORMATION OF S5 A DATA BREAK IN ANOTHER **CONTROL PATH CONTAINED** NULLIFY THE INFORMATION OF A IN THE EXCEPTION INHIBITING DATA BREAK IN ANOTHER CONTROL DATA BREAK HISTORY TABLE PATH CONTAINED IN THE EXCEPTION INHIBITING DATA BREAK HISTORY **TABLE** PERFORM A DATA BREAK **OPERATION** S13 **NULLIFY THE INFORMATION** OF A DATA BREAK IN A CONTROL PATH IN WHICH S14 ~ **EXECUTION IS ENSURED**

END

FIG.60

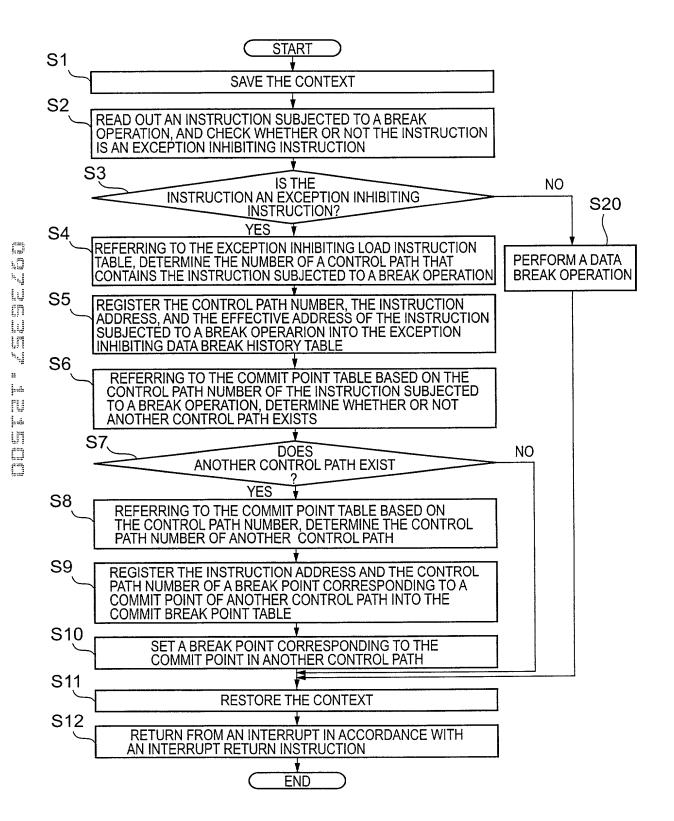


FIG.61

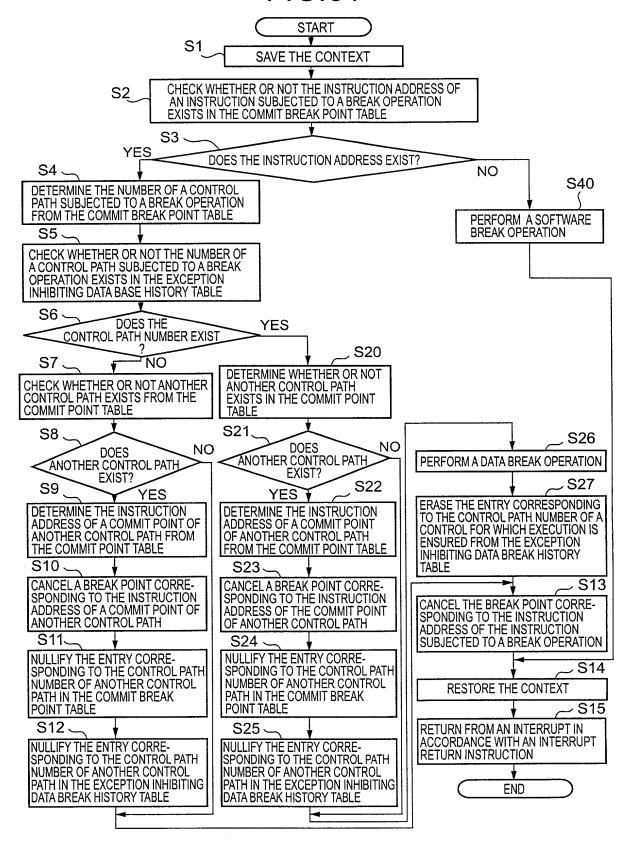


FIG.62

INSTRUCTION ADDRESS	PATH IDENTIFICATION NUMBER
а0	p0
a1	p1
:	:
:	:
ai	pi

FIG.63

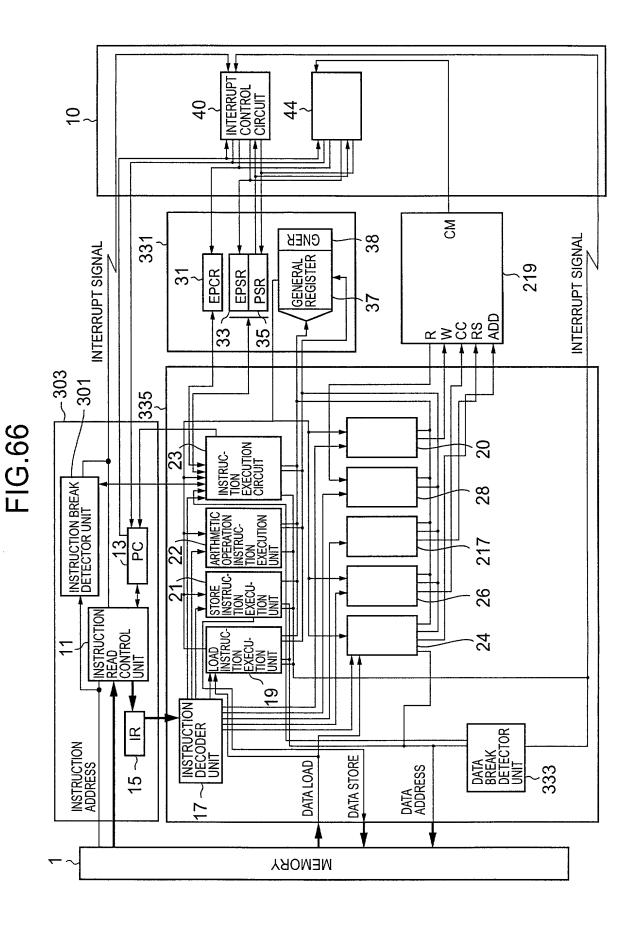
PATH IDENTIFICATION NUMBER	INSTRUCTION ADDRESS	ANOTHER PATH IDENTIFICATION NUMBER
p0	b0	sp0
p1	b1	sp1
:	:	:
:	:	:
рj	bj	spj

FIG.64

INSTRUCTION ADDRESS	PATH IDENTIFICATION NUMBER
b0	p0
b1	p1
:	:
:	:
bk	pk

FIG.65

PATH IDENTIFICATION NUMBER	INSTRUCTION ADDRESS	EFFECTIVE ADDRESS
p0	с0	ec0
p1	с1	ec1
:	•	
:	:	:
pl	cl	ecl





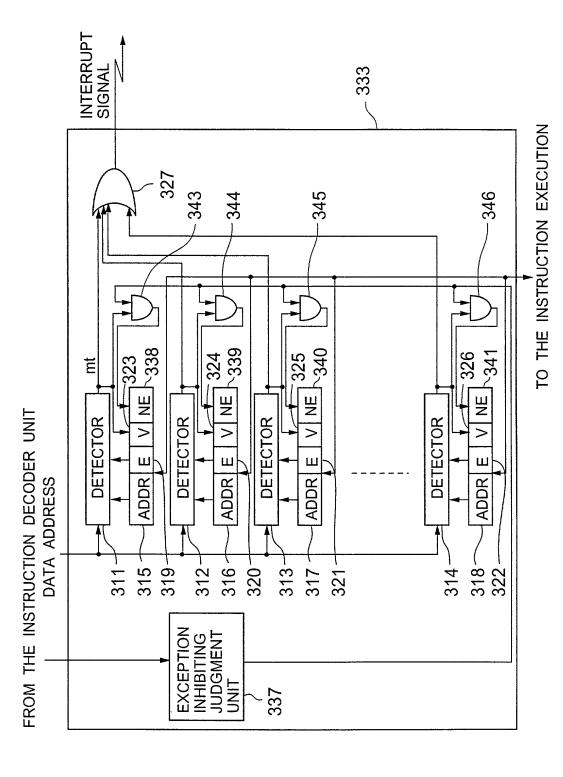


FIG.68

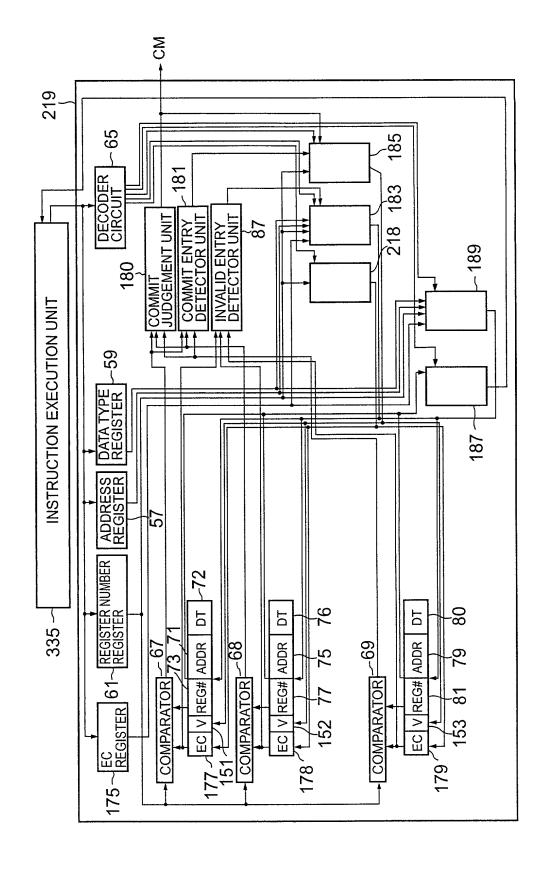
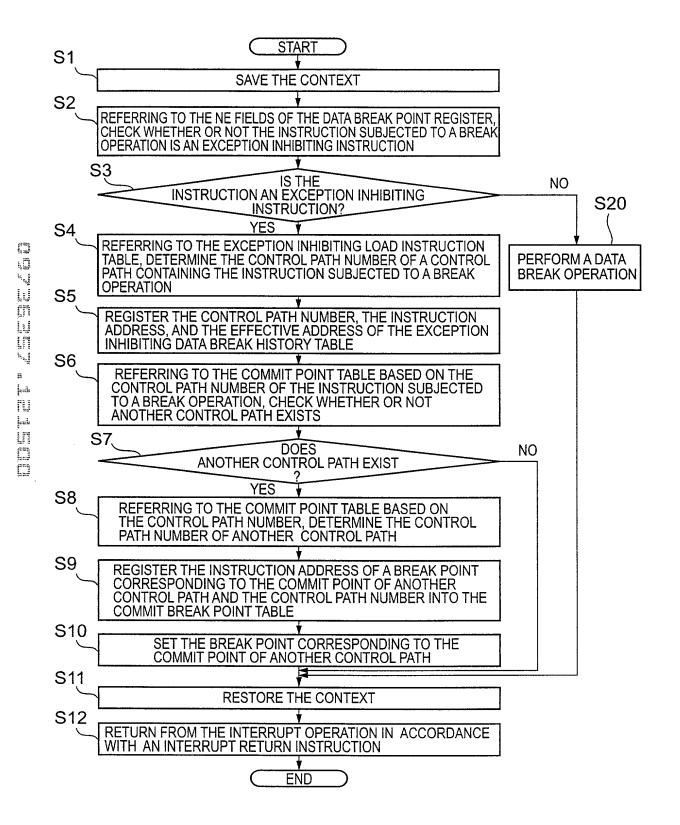


FIG.69



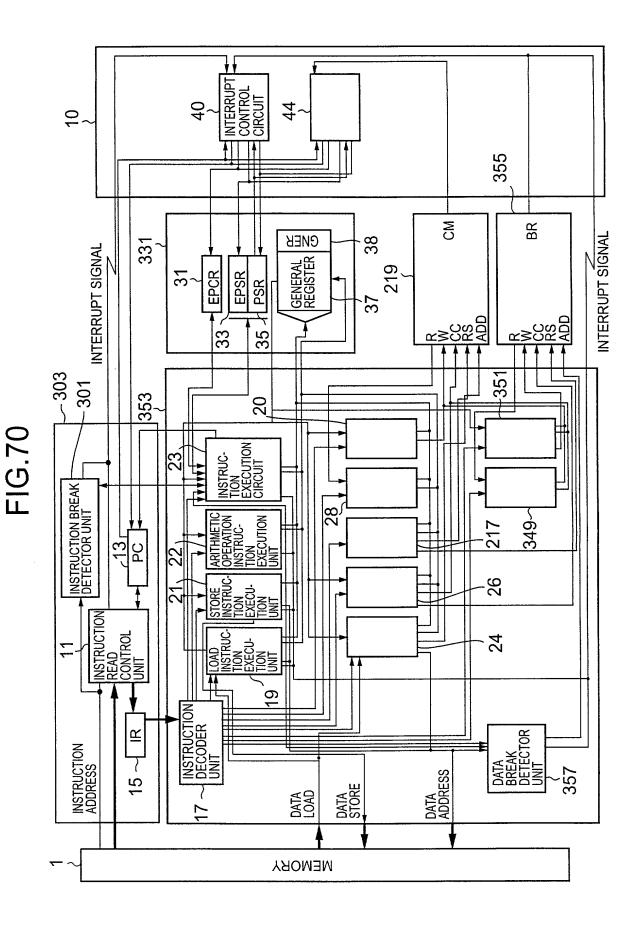


FIG.71

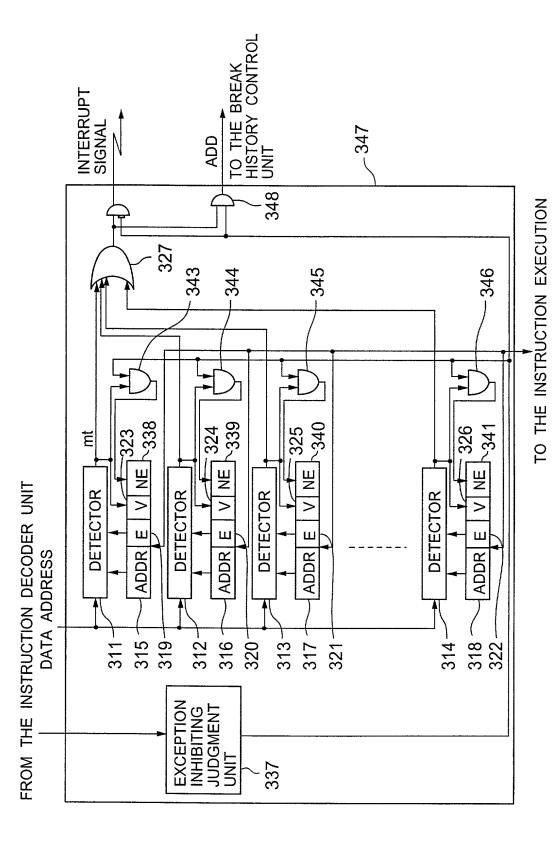
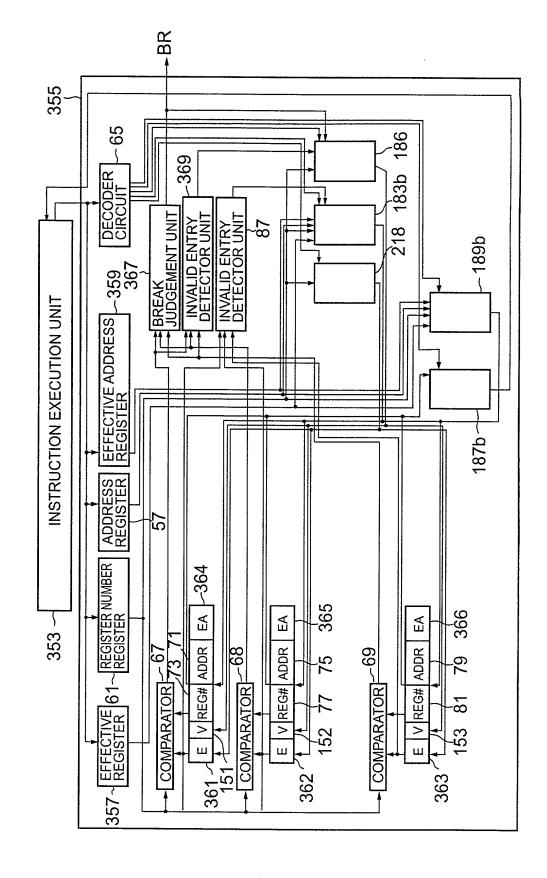


FIG.72



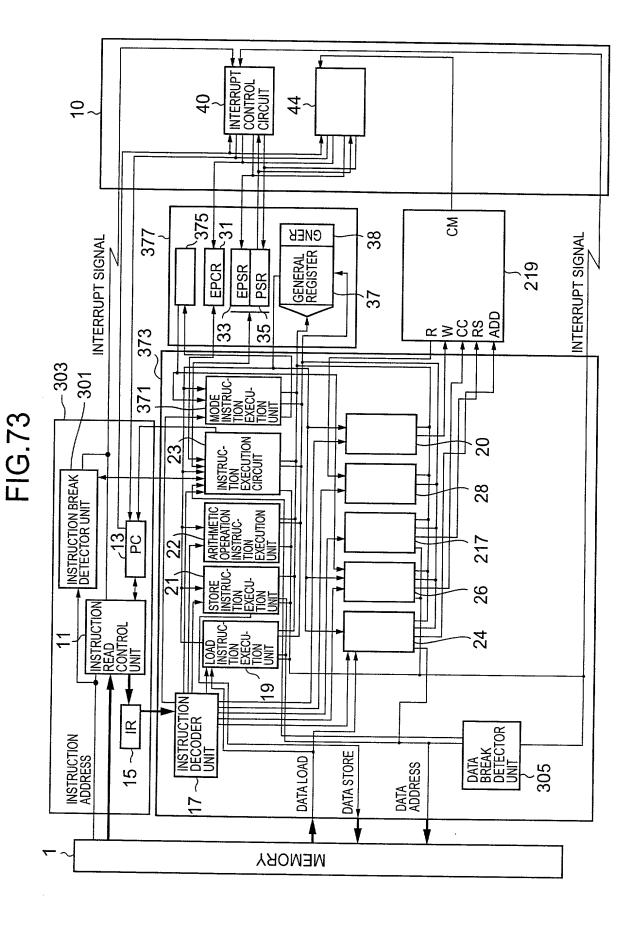


FIG.74

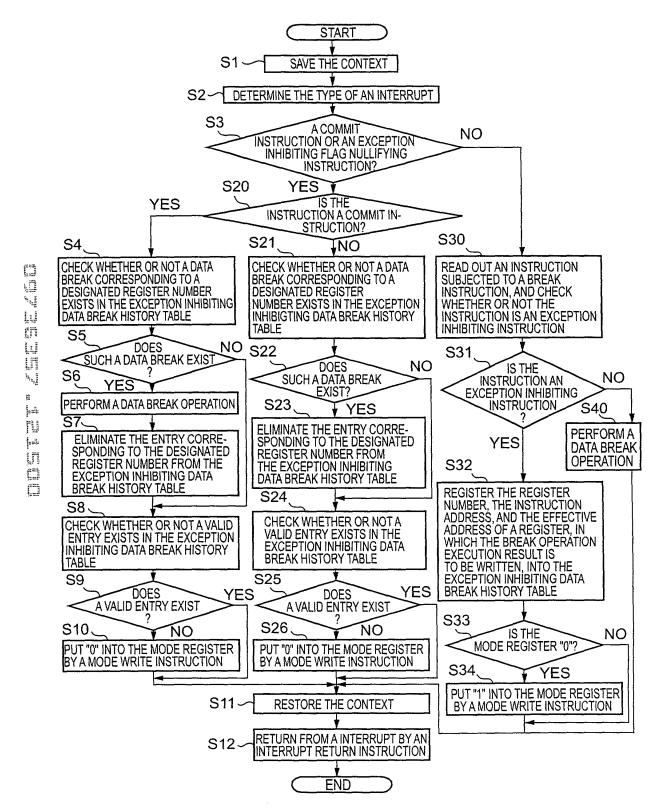


FIG.75

REGISTER NUMBER	INSTRUCTION ADDRESS	EFFECTIVE ADDRESS
r0	а0	ea0
r1	a1	ea1
:	:	:
:	:	:
rl	al	eal